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Scaled crystalline antimony ohmic contacts for two-dimensional transistors

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Transition metal dichalcogenides are a potential alternative to silicon and could be used to create transistors with a contacted gate pitch below 40 nm as required by the ångström-node transistor technology. However, it remains challenging to maintain an ohmic contact when the contact length is reduced to less than 20 nm. Here we show that crystalline semi-metallic antimony contacts can be epitaxially grown on molybdenum disulfide (MoS_2) by molecular beam epitaxy, creating ohmic contacts with a resistance of 98 Ω μm at a contact length of 18 nm. We use the contacts to build scaled field-effect transistors with a contacted gate pitch of 40 nm with drive currents of 0.85 mA μm^{-1}, 0.95 mA μm^{-1} and 1.08 mA μm^{-1} for monolayer, bilayer and trilayer MoS_2 channels, respectively. Statistical analysis of transistor arrays confirms that the crystalline antimony contacts are reproducible and stable.

It is increasingly challenging to continue scaling the size of silicon transistors while keeping power consumption low using complementary metal–oxide–semiconductor (CMOS) technology[1–4]. Transistor footprint is typically measured using the contacted gate pitch (CGP)—which is the sum of the gate length (L_g), contact length (L_c) and two spacer regions—as it is a more accurate figure of merit than L_g in evaluating the scaling potential of a transistor technology[5]. For example, silicon transistors produced at the 3-nm technology node have a CGP of 48 nm (ref. 6). The International Roadmap for Devices and Systems (IRDS) forecasts that CGP needs to reach 40 nm for the 1-nm node, with both L_g and L_c below 20 nm (ref. 7). Silicon transistors are scaled to such small dimensions that short-channel effects are severely exacerbated, degrading device performance. This has motivated the extensive exploration of alternative channel materials.

Two-dimensional (2D) transition metal dichalcogenides (TMDs), such as molybdenum disulfide (MoS_2), are, in theory, very suitable for making scaled transistors due to their atomic-scale thickness, large bandgap and immunity to short-channel effects[8–10]. Over the past

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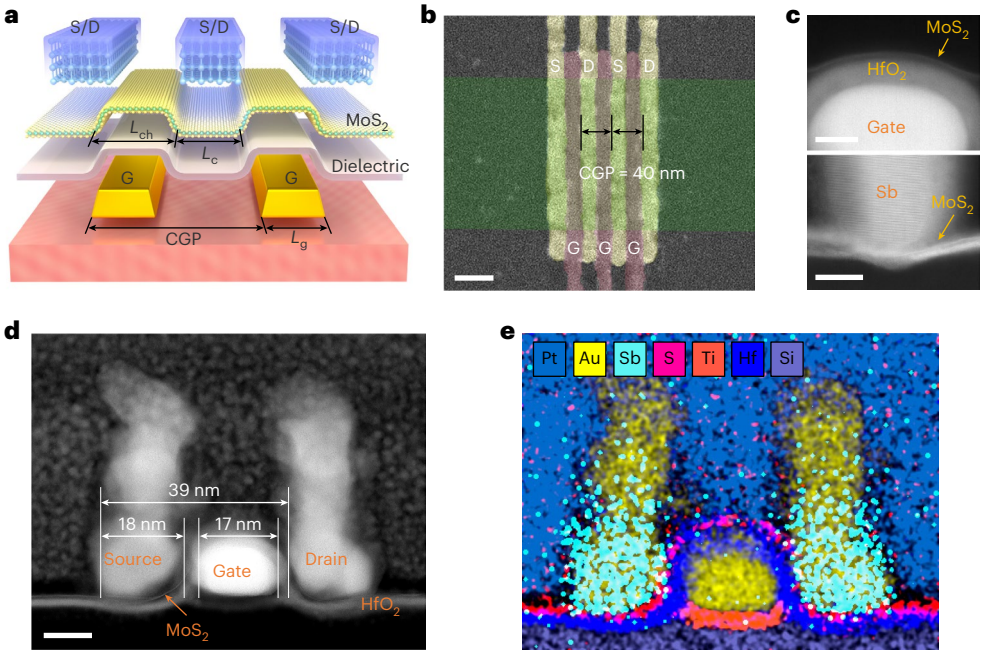

Fig. 1 | Scaling monolayer MoS_2 transistors to 40-nm CGP. a, Schematic of small-footprint transistors with monolayer MoS_2 channel. **b**, False-coloured SEM image of three local back-gated MoS_2 FETs in series with shared source/drain (S/D) contacts. A CGP of 40 nm is achieved with L_c = 20 nm and L_g = 20 nm. **c**, The HR-STEM characterization of the gate-stack and contact interfaces in our MoS_2 devices. The upper image shows the gate-stack structure containing MoS_2/HfO_2/gate with tight alignment and distinct boundaries. The lower image shows the scaled Sb–MoS_2 contact structure with sharp contact interfaces, in which the crystalline Sb (01$\bar{1}$2) electrodes exhibit clear lattice periodicity. **d**,**e**, Cross-sectional STEM image (**d**) and EDS map (**e**) of an as-fabricated sub-40-nm CGP MoS_2 transistor. It should be noted that the measurements of CGP, L_g and L_c presented here are all based on the vertical projected dimensions, in accordance with the established rules for standard silicon-based CMOS devices[7]. Scale bars, 50 nm (**b**), 5 nm (**c**, upper image) and 10 nm (**c**, lower image, and **d**).

decade, several milestones in field-effect transistors (FETs) with TMD channels have been reported[2,11–16], including the scaling of L_g down to around 1 nm while maintaining good switching characteristics[2,3]. However, these demonstrations showed devices with a much larger overall footprint than 40 nm or used global gating that cannot be adopted by the semiconductor industry. Typically, most reported high-performance TMD FETs focus on L_g scaling but have L_c in the range of hundreds of nanometres to micrometres[2,3,12,15,17–20].

A key challenge in 2D transistor scaling is the large increase in contact resistance (R_c) at highly scaled L_c dimensions[21,22]. The conventional metal silicide contact process, integral to silicon CMOS technology, cannot be applied to 2D materials due to the absence of surface dangling bonds and their ultra-thin nature. Despite efforts to address the contact issue in TMDs[15,21,23–26], such as using semimetal contacts (such as Sb, Bi and Sn)[12,13,27], the challenge of L_c scaling remains. Theoretically, maintaining low R_c at small L_c necessitates a small transfer length (L_T), which is the effective carrier injection length from contact to channel[21]. Technology computer-aided design simulations show that carrier injection predominantly occurs at the contact edge for TMDs[28]. Sub-20-nm contact length has been experimentally demonstrated using contacts made of Ni (ref. 29) and metallic carbon nanotubes (CNTs)[30], but they also exhibited R_c values exceeding 10 kΩ μm. For semi-metallic Bi and Sb contacts, nanometre-scale L_T was derived using the transmission line method (TLM) on devices with micrometre-scale contact lengths[12,13], which can produce large uncertainties and deviate substantially from the true value[23,31]. To the best of our knowledge, no contact deposition process has been reported that unambiguously delivers performance to the IRDS requirements at the 1-nm node[7].

In this Article, we report an ohmic contact technology for scaled MoS_2 FETs that uses crystalline Sb (01$\bar{1}$2) contacts grown using ultra-high-vacuum molecular beam epitaxy (MBE). The crystalline Sb contact achieves a R_c under 100 Ω μm at L_c = 18 nm, which fulfils the IRDS 1-nm node requirements. Technology computer-aided design simulations indicate that our crystalline Sb contact has a L_T of 13 nm and contact resistivity of 8.9×10^{-9} Ω cm. We fabricate MoS_2 FETs with 40-nm CGP that can deliver a drive current of more than 1 mA μm^{-1} under 0.6 V of drain voltage, while maintaining high electrostatic control, demonstrating excellent performance-power-area advantages compared with other reported MoS_2 FETs. We also conduct statistical measurements on over 50 FETs to illustrate the reproducibility and scalability of our crystalline Sb contact technology.

Crystalline Sb (01$\bar{1}$2) contact by MBE

Figure 1a shows the artistic illustration and relevant length scales of the MoS_2 FETs. The devices adopt a localized back-gate configuration, consisting of chemical-vapour-deposited monolayer MoS_2 channel[32], crystalline Sb (01$\bar{1}$2) contact and 3 nm HfO_2/2 nm Ti/8 nm Au high-κ metal gate stack. The fabrication processes are detailed in Methods and Supplementary Fig. 1. The scanning electron microscopy (SEM) image depicted in Fig. 1b of the closely packed MoS_2 transistor demonstrates a CGP of ~40 nm. Figure 1d presents a cross-section scanning transmission electron microscopy (STEM) image of a typical FET. The CGP is ~39 nm by measuring the edge-to-edge separation of the source and drain electrodes. The L_g and L_c are measured at 17 nm and 18 nm, respectively. The gate has little overlap with source–drain electrodes, which helps to reduce parasitic capacitance while eliminating the need for extension doping[14]. Moreover, the spatial distribution of Sb, Hf, Au, S and Ti elements in energy dispersive spectrometer (EDS) mapping further confirms the device structure (Fig. 1e). In addition, high-resolution STEM images (Fig. 1c) were used to conduct a magnified analysis of the critical interfaces of the MoS_2 FETs. Within the gate-stack configuration, the MoS_2, HfO_2 and gate were found to be in intimate contact with well-defined boundaries. Furthermore, even when the L_c were scaled down to below 20 nm, Sb maintained a close contact with MoS_2, exhibiting a crystalline orientation of (01$\bar{1}$2) (Fig. 1c and Supplementary Fig. 2).

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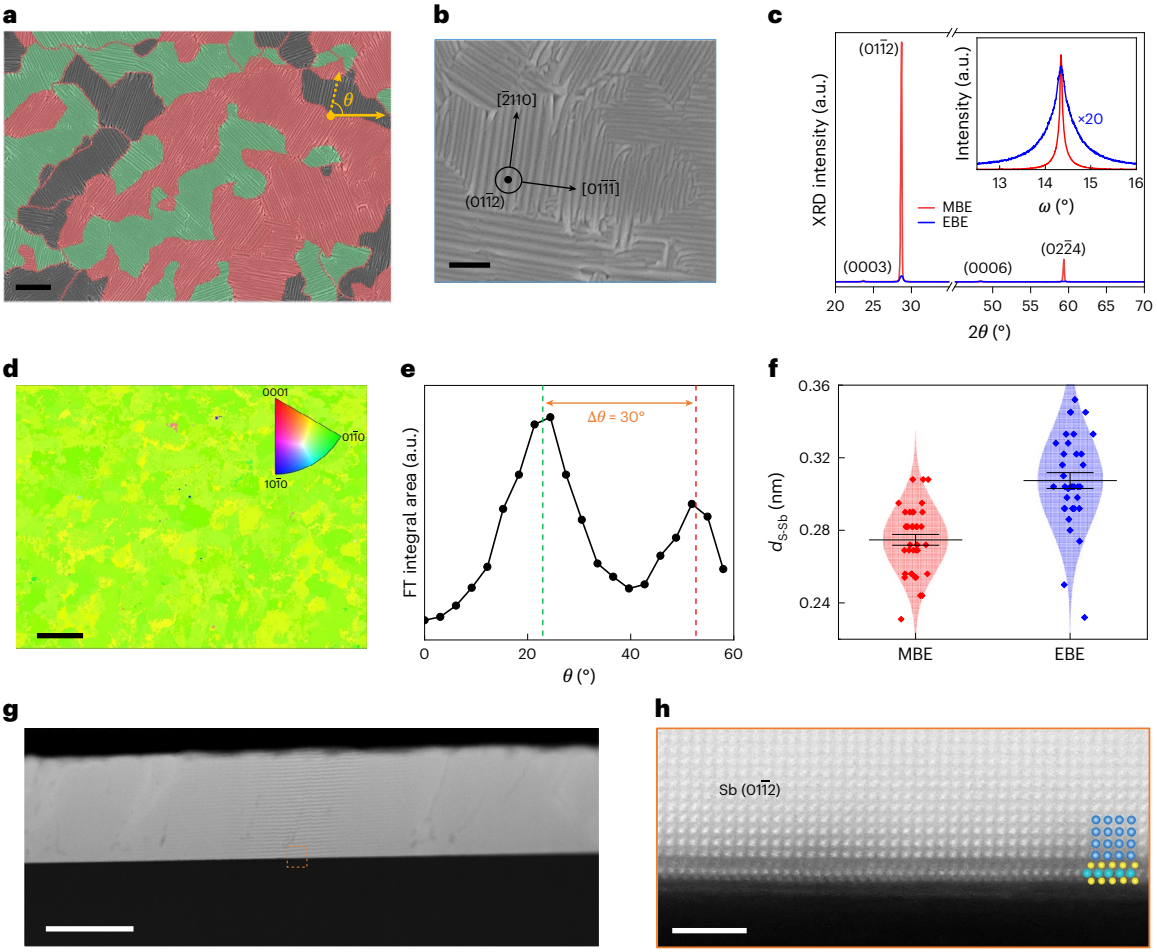

Fig. 2 | Characterizations of MBE crystalline Sb (01$\bar{1}$2). a, SEM image of the Sb film grown by MBE; the domain size was typically more than 1 µm. The angle (θ) is measured between the SEM bottom edge and the parallel direction of Sb grain stripes. The red and green false-colour areas represent the two epitaxial relationships in the period of 0–60° (MoS_2 has triple rotational symmetry, with 60° as the period), accounting for 48% and 33.7%, respectively, corresponding to the zigzag or armchair side of MoS_2. **b**, Zoom-in SEM image of the Sb film in **a**. The crystal orientations parallel and perpendicular to the stripes were <$\bar{2}$110> and <01$\bar{1}\bar{1}$>, respectively. **c**, XRD θ–2θ diffractogram of the Sb film by EBE (blue line) and MBE (red line). Inset: XRD rocking curves of the (01$\bar{1}$2) peak. 2θ is the angle between the incident X-rays and the detector and ω is the angle between the incident X-rays and the measured Sb films. **d**, EBSD *z* axis inverse pole figure mapping (normal to the sample surface) of the Sb film by MBE. **e**, Area distribution of all Sb domains in **a** calculated after Fourier transform (FT). **f**, Statistical distribution of the vdW distances between Sb and S in the Sb (01$\bar{1}$2)–MoS_2 contact prepared by two processes. The pink and light blue shaded outlines are Gaussian fitting. The centre of each distribution represents the mean value, and the error bars represent the standard deviation. The total sample sizes (n) were 38 for MBE Sb devices and 35 for EBE Sb devices. **g**, Cross-section HAADF-STEM image of the Sb (01$\bar{1}$2)–MoS_2 contact by MBE. **h**, Zoom-in atomic-resolution image from the orange dotted box in **g**. Scale bars, 500 nm (**a**), 200 nm (**b**), 1 µm (**d**), 100 nm (**g**) and 2 nm (**h**).

Our previous work showed that semi-metallic Sb (01$\bar{1}$2) could reduce the contact resistance of MoS_2 close to the quantum limit[12]. However, conventional electron-beam evaporation (EBE) only produces nano-crystalline or amorphous films without long-range crystallinity[33]. When L_c is below ~20 nm, that is, comparable to the grain size of the EBE films, the contact will be limited by the phase purity and crystallinity of Sb (01$\bar{1}$2) and inevitably show large variations. To optimize the Sb contact at extremely scaled L_c, we developed a deposition process using ultra-high-vacuum MBE (see Methods for details). Compared with EBE, MBE can achieve much better material and interface quality. First, operating in an ultra-high-vacuum environment (~10^{-7} Pa) effectively removes adsorbed molecules and impurities on MoS_2 and improves surface cleanliness. Second, it lowers the evaporation temperature and therefore the kinetic energy of the Sb source, which minimizes defect creation on deposition on the MoS_2 surface[24]. Third, MBE provides more precise control over deposition rate (<0.02 nm s^{-1}) and substrate temperature (±0.05 °C). This reduces the impact of growth kinetics and promotes the thermodynamically stable crystalline Sb (01$\bar{1}$2) on MoS_2 as supported by a set of characterizations (Fig. 2). In contrast to EBE, the Sb film grown by MBE showed stripe-like morphology under SEM, indicating crystalline Sb domains (Fig. 2a,b and Supplementary Fig. 3). STEM analysis of the closely and parallel-aligned stripes in Supplementary Fig. 4a indicates that they share identical lattice structure and orientation, confirming they belong to a crystalline domain. The domain size was typically several micrometres. Combining with the STEM data in Fig. 2h, we confirmed that the crystallographic plane in contact with MoS_2 was indeed Sb (01$\bar{1}$2) and that the orientations parallel and perpendicular to the stripes were <$\bar{2}$110> and <01$\bar{1}\bar{1}$>, respectively (Fig. 2b).

The high quality of crystalline Sb was further supported by X-ray diffraction (XRD) measurements (Fig. 2c). The in-plane XRD θ–2θ diffractogram displayed a dominant (01$\bar{1}$2) peak and its satellite (02$\bar{2}$4) peak. The (01$\bar{1}$2) peak intensity was 190 times higher than the (0003) peak, indicating highly crystalline and pure (01$\bar{1}$2) phase. The XRD rocking curve, a reliable measure of the out-of-plane tilt, showed a narrow full-width at half-maximum of 0.12° (Fig. 2c inset). In contrast,

Sb deposited by EBE showed much lower intensity and broader full-width at half-maximum (0.56°) in the θ–2θ and rocking curve scans, consistent with the nano-crystalline nature and low phase purity. To quantitatively measure the phase purity over a large area, we used electron backscatter diffraction (EBSD)[34]. In the experiment, a focused electron beam inside an SEM illuminated the Sb/MoS_2 sample at a 70° angle from the surface normal and the Kikuchi pattern was transformed into the crystallographic orientation map through statistical analysis. Figure 2d shows the inverse pole figure in the out-of-plane z-direction over a 50-μm^2 area. Nearly all the domains showed a yellow-green colour corresponding to $(01\bar{1}2)$. Note that the slight colour difference is due to the presence of an inclination angle in the ridge-like structure when Sb reaches a certain thickness (Fig. 2a,b). By calculating the green and yellow areas in the z axis inverse pole figure map, we derived the phase purity of Sb $(01\bar{1}2)$ to be 97.2%, which was consistent with the intensity ratio in XRD. In addition, the Sb film deposited on the 2-inch MoS_2 single crystal shows excellent wafer-scale uniformity and is suitable for large-scale device integration (Supplementary Fig. 5).

The crystalline Sb $(01\bar{1}2)$ on MoS_2 was epitaxial as revealed by artificial intelligence-assisted image analysis of the SEM images (Fig. 2a and Supplementary Fig. 6). By using automatic edge detection and Fourier transform techniques, we quantified the orientation distribution of Sb domains. Statistical analysis of the domain orientation showed a preference every 30° (Fig. 2e), indicating that the Sb stripes were not randomly oriented but preferably aligned with zigzag or armchair directions of MoS_2. The red and green colour coding in Fig. 2a illustrated the two preferred orientations, which exceeded 80% of the total area. The epitaxial relationship was further supported by cross-section high-angle annular dark-field STEM (HAADF-STEM). Figure 2g shows a HAADF-STEM image cut along the Sb $< 01\bar{1}\bar{1} >$ direction, that is, perpendicular to the stripes. We observed several Sb grains with ~300 nm lateral dimension corresponding to the width of each stripe. The grains were crystalline with the same lattice orientation, as indicated by the diffraction fringes. Atomic-resolution HAADF-STEM of several samples indeed showed that the Sb $< 01\bar{1}\bar{1} >$ was preferably aligned with the MoS_2 zigzag ($< 11\bar{2}0 >$) or armchair ($< 10\bar{1}0 >$) directions, confirming the epitaxial relationship (Fig. 2h and Supplementary Fig. 7a,b).

Atomic-resolution HAADF-STEM further revealed a pristine Sb–MoS_2 interface without metal-induced defects (Fig. 2h). The van der Waals (vdW) gap between the first layer of Sb atoms and MoS_2 appeared to be reduced in MBE crystalline samples. Statistical analysis of 36 locations showed that the average vdW distance for MBE crystalline Sb (0.272 nm) was nearly 11% smaller than that deposited by EBE (0.309 nm) (Fig. 2f and Supplementary Fig. 7). This could be attributed to the removal of surface contaminants under an ultra-high-vacuum environment. The reduced vdW gap led to enhanced band hybridization and charge transfer between Sb and MoS_2, as shown by density functional theory (DFT) calculations (Supplementary Fig. 8).

Electrical properties of MBE Sb $(01\bar{1}2)$ contact

First, the relationship between Sb deposition parameters and the contact quality of Sb–MoS_2 was systematically investigated. Substrate temperature (T_{sub}) was identified as a key factor. As shown in Fig. 3a, Sb forms an amorphous structure at room temperature. As the T_{sub} increases, the thermodynamic energy of Sb atoms on the MoS_2 surface is increased, promoting orderly atomic alignment and the formation of a densely packed crystalline Sb $(01\bar{1}2)$ thin film with large grain size. This greatly improves the contact quality of Sb–MoS_2, as evidenced by the I_{on} increase and R_c decrease in MoS_2 devices (Fig. 3b,c). Under T_{sub} = 88 °C (the highest temperature tolerable by our poly(methyl methacrylate) (PMMA) resist without lift-off failure), the average I_{on} (R_c) is increased (reduced) by 81% (87%) compared with room temperature. The deposition rate was found to be another critical parameter. Low-rate deposition also facilitates the crystallization of Sb, reduces surface roughness and promotes the growth of Sb $(01\bar{1}2)$-oriented grains, as revealed by SEM images in Supplementary Fig. 9c,d. In contrast, high-rate deposition leads to higher surface roughness and reduced phase purity of Sb $(01\bar{1}2)$, consistent with electrical measurements (Supplementary Fig. 9a,b). Although MBE is limited in large-scale device integration due to high cost, our findings provide valuable insights for the development of alternative fab-compatible technologies.

Next, we examined the electrical properties of the crystalline Sb contact using the optimized deposition conditions. To this end, we fabricated back-gated MoS_2 FETs with the same channel length L_{ch} = 100 nm but different L_c ranging from 1 μm to 20 nm. Figure 3d displays the transfer characteristics (drain current I_d versus gate voltage V_{gs}) of two representative FETs with L_c = 1 μm and 20 nm, respectively (inset is the SEM image of the device with L_c = 20 nm). The devices showed nearly the same on-state current. The output characteristics (I_d versus drain voltage V_{ds}) of the device with L_c = 20 nm showed good saturation behaviour and the saturation current reached 642 μA μm^{-1} under V_{ds} = 1 V (Fig. 3e). Statistical analysis of multiple FETs at each L_c showed nearly constant I_d independent of L_c down to 20 nm (Fig. 3f). For comparison, we fabricated FETs with the same dimension using EBE Sb contact[12]. The EBE Sb devices exhibited a 22% drop in I_d at L_c = 1 μm, which were also verified in the devices with the same structure as reported in ref. 12 (Supplementary Fig. 10a,b). Also, I_d continued to decrease with L_c scaling, indicating higher R_c than MBE crystalline Sb contacts (Fig. 3f and Supplementary Fig. 10c–f). Furthermore, we observed a large drop of I_d when L_c was below ~40 nm. The average I_d was reduced by 42.5% when L_c was scaled from 1 μm to 20 nm. Similar or more dramatic drops of I_d were invariably observed for Sb (ref. 16), Ni (ref. 29) and Au (refs. 18,35) contacts in the literature (Fig. 3f). For Ni and Au contacts, the transistor performance was severely limited by contacts at L_c = 20 nm, and the drive current was an order of magnitude lower.

To quantitatively obtain key parameters of the MBE crystalline Sb contact at ultra-scaled L_c, we used the distributed resistance network model[21]:

$$R_c = \sqrt{\rho_C R_{SH\text{-}C}}\coth\left(\frac{L_c}{L_T}\right);\quad L_T = \sqrt{\frac{\rho_C}{R_{SH\text{-}C}}} \tag{1}$$

where ρ_C is the specific contact resistivity, $R_{SH\text{-}C}$ is the sheet resistance under source and drain electrode, and L_T is the transfer length. It can be seen that R_c starts to increase exponentially when $L_c \le L_T$ due to the current crowding effect. Therefore, L_T can provide a quantitative assessment of the contact scaling potential. We used the rigorous TLM to extract R_c at different L_c (Fig. 3g and Supplementary Figs. 11 and 12). At L_c = 1 μm, the R_c of a hero device reached 25 Ω μm under a carrier concentration of 5.0×10^{13} cm^{-2} (Supplementary Fig. 11a). This was 40% lower than the previous record for a Sb $(01\bar{1}2)$ contact[12] (Supplementary Fig. 13b). A negative Schottky barrier height of −5 meV was derived by the flat-band model, which provided clear evidence for an ohmic contact (Supplementary Fig. 14). When L_c was scaled to 20 nm, the I_d of the MoS_2 FETs still showed strong dependence on L_{ch} (Supplementary Fig. 11d,e), indicating that the devices were not contact limited. On the basis of TLM, R_c = 98 Ω μm was derived at L_c = 18 nm, which compares favourably against other reported methods[5,16–18,30,35–37] (Fig. 3g). The confidence of the above R_c was confirmed by measuring additional TLM devices containing multiple sub-100-nm channel lengths and high correlation coefficients (R^2) close to 1 derived from the fitting process for L_c = 18 nm, 20 nm and 1 μm (Supplementary Fig. 11b–f). To further check the accuracy of R_c extracted by the TLM method, the Y-function method[23] was used and gave similar results (Supplementary Fig. 15).

To demonstrate the technology advancement[12,13,38], the R_c is plotted as a function of n_{2D} for deeply scaled $L_c \le 20$ nm in Fig. 3h. Our MBE crystalline Sb contact exhibits an R_c = 85 Ω μm, which is nearly an order of magnitude lower than the previous reports in the literature[16,37] and

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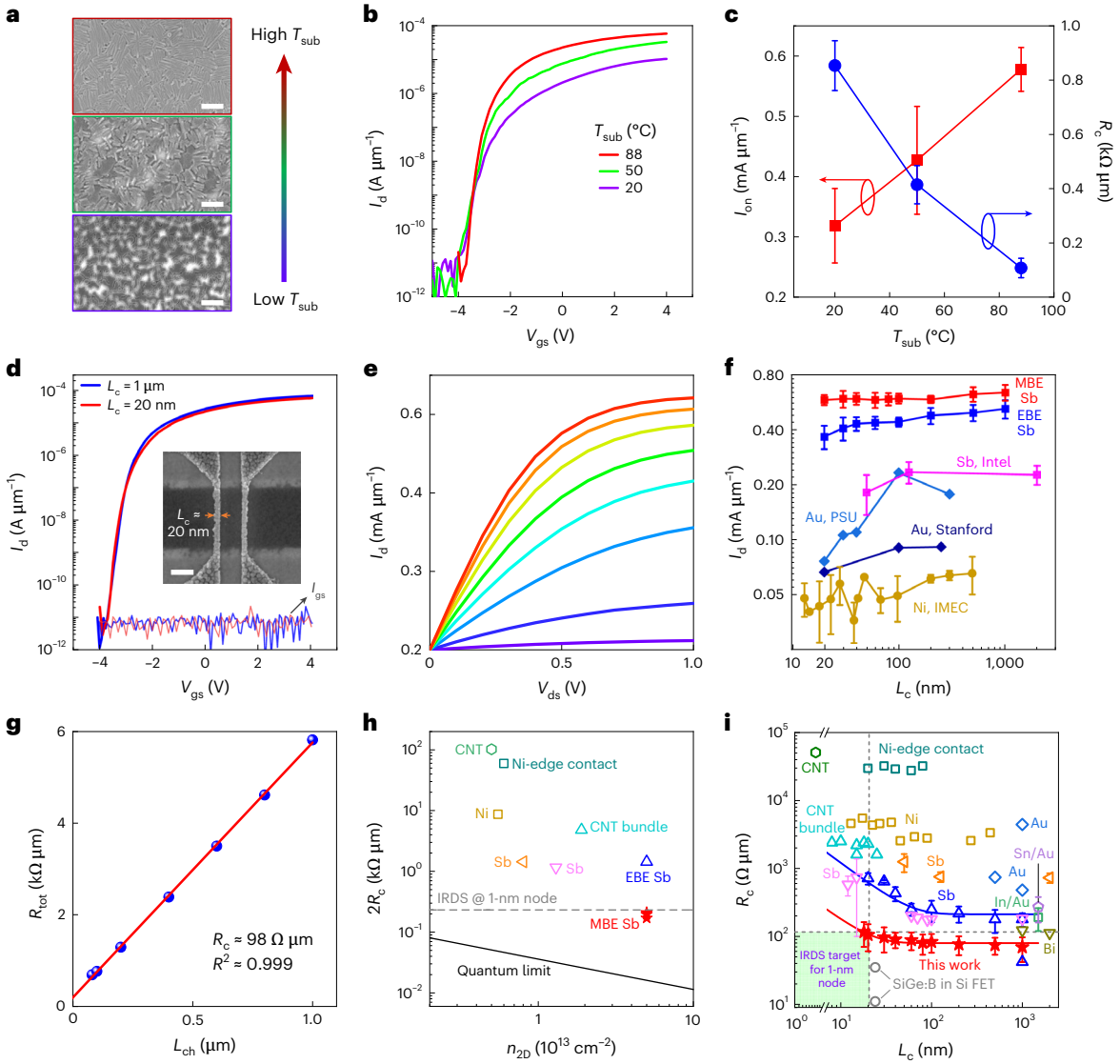

Fig. 3 | L_c scaling of MBE Sb ($01\bar{1}2$)–MoS_2 contact. a, SEM images of Sb films deposited on MoS_2 at different T_{sub} during the MBE deposition process. **b**, Transfer curves of MoS_2 transistors with MBE Sb contact fabricated at different T_{sub} corresponding to **a**, with V_{ds} = 50 mV. **c**, Variation trends of I_{on} (red symbols) and R_c (blue symbols) for MoS_2 transistors with MBE Sb contact fabricated at different T_{sub}. In each distribution, the central point corresponds to the mean value, while the error bars quantify the standard deviation (n = 12). **d**, Transfer characteristics and gate leakage current curve of a typical MoS_2 FET with L_c = 20 nm (red line) and L_c = 1 μm (blue line) under V_{ds} = 50 mV. Both devices have the same L_{ch} of 100 nm. Inset: SEM image of the 20 nm L_c device. **e**, Output characteristics of the same device in **d** with L_c = 20 nm. From bottom to top, V_{gs} = −1 V to V_{gs} = 6 V with 1-V steps. **f**, Benchmark of MoS_2 FETs I_d versus L_c with different contact metals (Sb (ref. 16), Ni (ref. 29) and Au (refs. 18,35)) at V_{ds} = 1 V. All devices have 100-nm L_{ch} except Ni contact reported by IMEC (L_{ch} = 29 nm) and Au contact reported by Stanford (L_{ch} = 40 nm). The centre point and error bars of each distribution represent the mean and standard deviation, respectively. For MBE Sb devices, n was 80, 14, 14, 14, 13, 13, 12, 10 and 8 as L_c decreased from 1 μm to 20 nm. For EBE Sb devices, n was 80, 14, 14, 13, 12, 12, 10 and 8 as L_c decreased from 1 μm to 20 nm. PSU, Pennsylvania State University. **g**, R_c extraction using the TLM method from the devices with L_c = 18 nm in Supplementary Fig. 11f. The y intercept and x intercept represent $2R_c$ and $2L_T$, respectively. R_{tot}, the total resistance of the device. **h**, The R_c as a function of n_{2D} in monolayer MoS_2 transistors for different contact techniques with contact lengths ≤20 nm (refs. 12,16,17,30,36,37,39). **i**, State-of-the-art contact technology for monolayer MoS_2 transistors plotted as a function of L_c (refs. 5,12,13,16–19,25,30,35–37,39–41). The solid line represents the fitting result via equation (1). Each distribution is characterized by a centre point (mean) and error bars (standard deviation). For MBE Sb devices, n was 15, 14, 14, 14, 13, 13, 12, 12, 11 and 9 as L_c decreased from 1 μm to 18 nm. For EBE Sb devices, n was 15, 14, 14, 13, 12, 12, 10 and 7 as L_c decreased from 1 μm to 20 nm. Scale bars, 200 nm (**a**) and 100 nm (**d**).

meets the target for the IRDS 1-nm node[7]. In Fig. 3i, we plotted R_c versus L_c for both MBE and EBE Sb contact, along with the available literature data on MoS_2 FETs[5,12,13,16–19,25,30,35–37,39–41]. Our R_c was not based on a single hero device but instead was an average of multiple devices at each L_c, and the variations are reflected by the error bars. We used equation (1) to fit the experimental data (solid lines in Fig. 3i) and derived L_T = 16.8 nm and 56.5 nm for MBE and EBE Sb contacts, respectively. In parallel, we established a technology computer-aided design device model[42] based on the TLM devices with L_c = 20 nm (Supplementary Fig. 16, see Methods for details), and L_T extracted from the current density contour in the Sb–MoS_2 contact region was ~13 nm, which is verified with equation (1) fitting the results in Fig. 3i. This demonstrates that our MBE crystalline Sb contact has convincing advantages in transistor scaling. Furthermore, the ρ_C of the MBE crystalline Sb contact was nearly an order of magnitude lower than that of EBE Sb (8.9×10^{-9} Ω cm^2 versus 1.2×10^{-7} Ω cm^2). It is notable that this value is two orders of magnitude lower than a typical Au–MoS_2 contact[18] and comparable to a chemically bonded Si–silicide contact[43].

In Fig. 3i, we comprehensively benchmark against existing contact methods[5,12,13,16–19,25,30,35–37,39–41]. For most studies demonstrating R_c approaching the IRDS target (the horizontal dashed line), such as Bi (refs. 13,44), Sb (ref. 12), Sn/Au (ref. 19) and In/Au (refs. 19,25), L_c was on the micrometre scale and no data were reported at scaled L_c. Some methods, such as edge and top Ni contacts[17,39], showed relative independence of R_c on L_c down to 13 nm. However, the R_c was several orders of magnitude higher. While CNTs[30] and CNT bundles[36] contacts were capable of achieving extremely small L_c, they showed very high R_c and their preparation methods were not compatible with large-scale device integration. It should be emphasized that although Sb is one of the most promising recent contact materials for MoS_2, its scaling potential to 20 nm has not been experimentally demonstrated. The pink triangles in Fig. 3i represent Taiwan Semiconductor Manufacturing Company's recent results on Sb contact[5,37], which almost coincide with our EBE process. The overall assessment is that EBE Sb is unlikely to satisfy the requirement for the 1-nm technology node because R_c increases steeply below 40 nm, consistent with the derived L_T = 56.5 nm. In contrast, MBE crystalline Sb (01$\bar{1}$2) maintains sub-100 Ω μm R_c down to 18 nm and falls into the desirable zone in terms of contact scaling (the green corner in Fig. 3i).

High-performance MoS_2 FETs scaled to 40-nm CGP

We combined contact and channel length scaling together to fabricate MoS_2 FETs with 40 nm CGP (Fig. 4a and Supplementary Fig. 1). Both L_c and L_g were designed to be 20 nm and the HfO_2 gate dielectric was 3 nm thick, corresponding to ~0.8 nm equivalent oxide thickness. Further breakdown testing of HfO_2 revealed low leakage current and high breakdown voltage to ensure reliable device operation (Supplementary Fig. 17a,b). Figure 4b,c and Supplementary Fig. 18 show the electrical performance of three representative FETs, with monolayer (1L), bilayer (2L) and trilayer (3L) MoS_2 as the channel materials, respectively. For the monolayer MoS_2 device, it exhibited steep subthreshold swing (SS) = 76 mV dec^{-1}, drain-induced barrier lowering (DIBL) of 20 mV V^{-1}, hysteresis <10 mV, on/off ratio >10^7 and leakage current <100 pA μm^{-1} under V_{ds} = 0.5 V. The small DIBL is not due to charge trapping effects as supported by the near-zero hysteresis in double-sweep measurements. The excellent low-power performance proves that MoS_2 has better short-channel immunity at the scaling limit than Si and CNTs. In terms of on-state performance, the FET showed full saturation at V_{ds} = 0.6 V with an on-state drive current of 850 μA μm^{-1}. The total on-state resistance was 315 Ω μm as extracted from the low-bias regime. This value was then subtracted by the channel resistance (calculated from Fig. 3e) to yield R_c = 105 Ω μm, which was in excellent agreement with TLM results. When the thickness of MoS_2 is increased to 2L and 3L, our MoS_2 devices exhibit superior consistency in on/off ratio, hysteresis and DIBL compared with monolayer devices. However, the SS and V_{th} experience slight degradation and leftward shift, respectively, due to the reduced gate control over the thicker channel. Notably, the output curves in Fig. 4c reflect a pronounced augmentation in the I_{on} for 2L and 3L MoS_2, reaching 0.95 mA μm^{-1} and 1.08 mA μm^{-1}, respectively. This improvement is attributed to the higher carrier concentration and mobility in 2L and 3L MoS_2 (refs. 45,46). These results clearly demonstrate the superior performance of small-footprint transistors fabricated using our MBE crystalline Sb contact technology. More electrical data for MoS_2 FETs with 40-nm CGP are presented in Supplementary Fig. 19. Besides, it should be noted that the MoS_2 transistor under investigation operates in depletion mode. To modulate the V_{th}, one can selectively use metal gates with varying work functions (Supplementary Fig. 20).

We benchmark these device performances with Si CMOS[47–49] and CNT FETs at a scaled footprint. We first compare the SS (Fig. 4e), which is a crucial parameter reflecting the low-power performance. The SS of our MoS_2 FETs with 40 nm CGP ranges from 62 mV dec^{-1} to 76 mV dec^{-1} (Fig. 4b and Supplementary Fig. 19), which approaches the theoretical Boltzmann limit. The SS is substantially lower than global back-gated MoS_2 FETs under similar channel lengths reported by the Interuniversity Microelectronics Centre (IMEC)[29] and CNT FETs[50] under the same CGP reported by IBM. Intel's 7–22 nm FinFET[47–49] has a similar SS but at a larger CGP, and there are no known solutions to maintain such a small SS at 40-nm CGP[7]. It should be emphasized that our comparison primarily focuses on metal–oxide–semiconductor FET devices (Supplementary Fig. 13a). While emerging concepts such as tunnelling, Dirac-source and negative-capacitance FETs can achieve sub-60 mV dec^{-1} SS, they face challenges in terms of performance and manufacturing[51–55].

We next analysed the on-state current and the off-state current of different transistor technologies with CGP less than 100 nm (refs. 47,48,50,56–58) (Fig. 4f). Our MoS_2 FETs exhibit an off-state current below 100 pA μm^{-1}, which surpasses Si FinFETs (>1 nA μm^{-1}) and CNT FETs (>100 nA μm^{-1}) and satisfies the IRDS high-density requirement[7]. The ultra-low static power dissipation is a key advantage of MoS_2 compared with Si and small-bandgap CNTs at 40-nm CGP. At on-state, our MoS_2 FETs exhibit slightly lower current compared with Si and CNT. However, we note that Si used very tall fins or multiple nanosheets to boost the on-state current, and that CNT achieved high current at the price of off-state leakage due to tunnelling through the small bandgap[50]. Nevertheless, the drive current of ultra-scaled MoS_2 FET still exceeds the IRDS high-performance requirement (753 μA μm^{-1})[7]. As future 1-nm node transistors will probably adopt a multilayer stacked channel, the on-state current will be proportionally increased.

To highlight the potential for large-scale integration, we extended our study to MoS_2 transistor arrays (Fig. 4g,h). Figure 4g shows the transfer characteristics of 54 MBE and 25 EBE MoS_2 FETs, all under 40-nm CGP. Analysis of the cumulative distribution functions of key parameters indicates that the I_{on} of MBE crystalline Sb-contacted MoS_2 devices is nearly 100% higher than that of EBE Sb-contacted devices, as shown in Fig. 4h (Supplementary Fig. 19). The device-to-device variation of I_{on}, SS and V_{th}, defined as the ratio of the standard deviation to the mean value, is similar for both processes. This suggests that for ultra-scaled MoS_2 FETs, the overall fabrication process, rather than the specific Sb deposition technique, is the primary source of variation. To further enhance device performance and reliability, it is essential to conduct design-technology co-optimization on key elements, such as the gate oxide, MoS_2 channel, contacts and doping, in conjunction with device design and simulation[59]. The reliability of our MoS_2 transistors was also evaluated in Supplementary Fig. 17. As shown in Supplementary Fig. 17c–e, after up to 500 repeated in situ measurements, a typical MoS_2 FET was still able to exhibit nearly the same transfer characteristics as the initial state without any degradation of I_{on} and I_g, demonstrating their robust reliability. To verify the environmental stability, a PMMA/HfO_2 bilayer encapsulation technique was developed. As illustrated in Supplementary Fig. 21a, the performance of our MoS_2 FETs in air after encapsulation closely mirrors that in vacuum before encapsulation, with negligible differences observed in hysteresis, I_{off} and I_{on}. Slight variations in SS and V_{th} are attributed to the inevitable residual interfacial doping. Furthermore, 100 repeated measurements conducted in air confirm the remarkable stability of the MoS_2 FETs in terms of transfer and output characteristics (Supplementary Fig. 21b–d). Collectively, these results demonstrate the reliability and stability of our MoS_2 devices under ambient conditions when properly encapsulated.

Conclusion

We have shown that MoS_2 FETs can be scaled to 40-nm CGP—reaching the 1-nm node performance target set by IRDS—by using crystalline Sb (01$\bar{1}$2) deposited by MBE to create ohmic contacts at small contact lengths. The contacts can achieve a R_c of 98 Ω μm at L_c of 18 nm. Monolayer and trilayer MoS_2 FETs created using these contacts with a CGP of 40 nm can exhibit a drive current of 0.85 mA μm^{-1} and 1.08 mA μm^{-1} at 0.6 V of drain voltage, respectively. Our results validate the scaling potential of 2D semiconductors in the context of ångström-node transistor technology.

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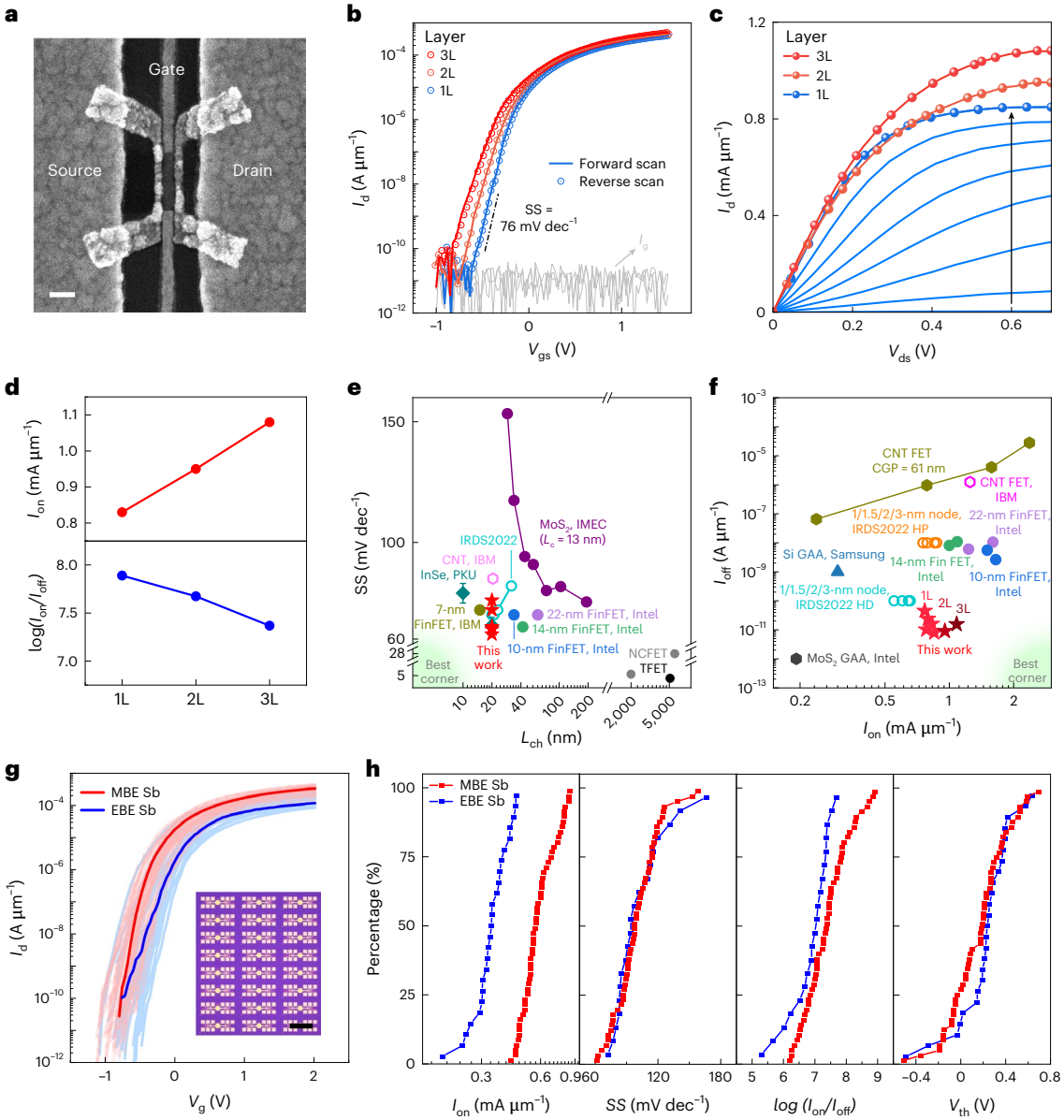

Fig. 4 | Electrical performance of MoS_2 FETs with 40-nm CGP. a, SEM image of a typical MoS_2 FET with CGP = 40 nm, L_c = 20 nm, L_g = 22 nm and L_{ch} = 19 nm. **b**, Transfer characteristics of the 1L (blue line) to 2L (orange line) and 3L (red line) MoS_2 device under V_{ds} = 0.5 V. SS, switching on/off ratio and DIBL of the monolayer MoS_2 device are 76 mV dec^{-1}, over 10^7 and 20 mV V^{-1}, respectively. **c**, Output characteristics of the same device in **b**. From bottom to top, V_{gs} = 0 V to V_{gs} = 3.5 V with 0.5 V steps. **d**, The variation trends of I_{on} and on/off ratio for 40-nm CGP MoS_2 FETs as the MoS_2 channel thickness increases from 1L to 2L or 3L. The data for the 2L and 3L MoS_2 devices are from Supplementary Fig. 18. **e**, Benchmark of SS versus L_{ch} for monolayer MoS_2 and other semiconductors in the literature[15,29,47–53], for CGP ≤200 nm. Solid symbols and empty symbols represent experimental results and predicted results, respectively. **f**, Benchmark of I_{off} versus I_{on} within 100-nm CGP for monolayer MoS_2 and other semiconductors in the literature[47,48,50,56–58], in which the calculations of I_{on} were performed using the effective channel width, in line with standard practices[7]. The dark yellow hexagons represent a 60-nm CGP CNT FET[56] under a series of V_{ds} voltages, including 0.1 V, 0.3 V, 0.5 V and 0.8 V from left to right. The specific CGP values corresponding to other FETs can be obtained from the same colour symbols in **e**. Note that all the performance comparisons for transistors of different materials and technologies are based on the CGP measured in the vertical projection dimension as a variable. **g**, Transfer characteristics of 54 MBE crystalline Sb-contacted (red lines) and 25 EBE Sb-contacted (blue lines) MoS_2 FETs with 40-nm CGP under V_{ds} of 0.5 V. Inset is an optical microscope image of small-footprint MoS_2 FET arrays fabricated on a SiO_2/Si substrate. **h**, Cumulative distribution function plots of key device metrics, including I_{on}, SS, on/off ratio and V_{th}. For MBE crystalline Sb-contacted MoS_2 FETs, the mean values of I_{on}, SS, V_{th} and on/off ratio are 596.2 μA μm^{-1}, 99.5 mV dec^{-1}, 0.16 V and 2.4 × 10^7, respectively. Scale bars, 50 nm (**a**) and 400 μm (**g**).

Methods

Growth and transfer of MoS_2 single crystals

Monolayer MoS_2 single-crystal film was synthesized using a previously reported method using a specially designed C/A-plane sapphire substrate[32]. The substrate featured a cutting angle ranging from 0.2° to 1°. Before the growth, the substrates were subjected to a low-pressure annealing process at 1,000 °C for 4 h. This process was conducted under a gas flow comprising 400 sccm of Ar and 100 sccm of O_2, facilitating the formation of uniform steps essential for the unidirectional alignment of MoS_2 domains. The MoS_2 growth occurred in a customized chemical-vapour-deposition furnace under low-pressure conditions. A silica crucible, containing 30 g of elemental sulfur powder, was independently heated to a temperature range of 180–200 °C and the sulfur was transported using a 300-sccm flow of Ar. High-purity molybdenum

pellets served as the molybdenum source and were carried by a 3-sccm flow of O_2 to form MoO_3. This MoO_3 was then conveyed separately from the sulfur source into the growth chamber, using a 100-sccm flow of Ar. For the synthesis of bilayer and trilayer MoS_2 films, the above monolayer MoS_2 single crystal was used as the growth substrate. The growth was performed at temperatures ranging from 850 °C to 1,000 °C for durations of 30 min to 60 min. The nucleation of 2L and 3L MoS_2 was promoted by increasing the Mo precursor concentration via elevated source temperatures, thus enabling layer-by-layer growth of the films[60].

The transfer of MoS_2 was executed using a polymer-based method. Initially, PMMA (Allersist, 950 K) was spin-coated onto the MoS_2/sapphire wafer at 2,000 rpm and subsequently baked at 150 °C. Following this, a thermal release tape was laminated onto the surface and used to delicately detach the PMMA/MoS_2 stack from the sapphire substrate in a KOH solution. The thermal release tape/PMMA/MoS_2 stack was then transferred onto the target substrate and baked at 120 °C to facilitate release of thermal release tape. Finally, the PMMA layer was dissolved using acetone.

Device fabrication process of MoS_2 FETs

First, electron-beam lithography (EBL), using PMMA A4, 950K as a photoresist, defined metal markers and back-gate pads on a 275 nm SiO_2/heavily doped silicon substrate. This was followed by EBE of 4 nm/50 nm Ti/Au and subsequent lift-off. The process of EBL and EBE was repeated to fabricate thin gate electrodes of 2 nm Ti/8 nm Au, using PMMA A2, 450K as the photoresist. Surface treatment to remove organic contaminants was conducted for 30 s using an inductively coupled plasma emission spectrometer. Subsequently, the substrate was promptly transferred to a chamber for atomic layer deposition. Atomic layer deposition (using Beneq TFS 200) of a 3-nm-thick HfO_2 back-gate layer on the substrate was carried out at 150 °C, using O_2 plasma as the oxygen source. MoS_2 films were then transferred onto the prepared substrate using the above method and subsequently etched into a banded structure, using PMMA as a mask. The source and drain contacts were defined through two distinct steps. Initially, PMMA A4, 950K was spin-coated at 4,000 rpm and subsequently baked at 150 °C for 8 min to dry. Pads were defined using EBL, followed by EBE of 4 nm/40 nm Ti/Au and lift-off. Subsequently, thinner PMMA A2, 495K was spin-coated at 4,000 rpm and postbaked at 150 °C for 8 min. Electrodes were designed to feature a narrow linewidth and a small pitch. Factors including beam current, exposure dose and development time greatly affect exposure quality. The electrode was exposed to a 0.2-nA beam current, and the PMMA was developed for 3 min in a low-temperature (~8 °C) developer and isopropyl alcohol. The effective removal of PMMA in the exposed MoS_2 regions is influenced by several key factors, including the low-temperature storage and use of PMMA solution, the stable control of the beam current during EBL and the precise low-temperature development process. The atomic force microscopy characterization of the MoS_2 surface postdevelopment and pre-Sb deposition (Supplementary Fig. 22) reveals that the MoS_2 surface, following the EBL process, exhibits a pristine and residue-free morphology, thereby facilitating the crystalline deposition of Sb with enhanced efficacy. Subsequently, 8–20 nm Sb was evaporated at a slow rate in our high-vacuum MBE chamber, followed by the evaporation of 10–30 nm Au at a 0.15 Å s^{-1} rate in the EBE chamber (10^{-9} torr) and lift-off. The working distance between the evaporation crucible and the substrate in the MBE system is set to about 55 cm to enhance the uniformity of the Sb film, aligning with the 60-cm distance used in the EBE system. Nitrogen was used to protect the samples during transport to the MBE chamber. It should be noted that the thorough removal of PMMA at the exposed MoS_2 region, as well as factors such as the high-vacuum environment, precisely controlled temperature and an appropriate evaporation rate during the deposition process are extremely crucial for the formation of nano-crystalline contacts. It is worth noting that the above procedure is for the preparation of small-sized MoS_2 transistors. If TLM devices with different contact lengths are prepared, only appropriate adjustments to the layout and process steps are required.

Characterizations

XRD and rocking curves were performed on a Bruker D8 Discover system. The SEM images were captured using a ZEISS EUV SEM operating at 5 kV. EBSD patterns were acquired using a Symmetry EBSD detector from Oxford Instruments on a Zeiss Sigma SEM at 20 kV, with the sample tilted at 70°, and were analysed using the Aztec and Channel 5 software. Cross-section transmission electron microscopy sample preparation entailed milling the sample with a focused ion beam, specifically the FEI Helios Nanolab G3 CX. Before milling, a 30 nm amorphous carbon layer was deposited on the sample surface. A rectangular area adjacent to the crystal grain was chosen, followed by the deposition of 700 nm and 1 µm of Pt to safeguard the sample at 5 kV, 0.17 nA and 30 kV, 80 pA, respectively. The milling process used a gallium ion source at 30 kV, 0.79 nA for regular milling and 5 kV, 7 pA for fine-tuning the cross-section. STEM images were captured with a FEI Titan Themis, equipped with an X-FEG electron gun and a DCOR aberration corrector, operating at 300 kV. For STEM imaging and EDS analysis, inner and outer collection angles (β_1 and β_2) of 48 mrad and 200 mrad, respectively, and a probe convergence semi-angle of 25 mrad were used. The beam current for HAADF imaging and EDS chemical analyses was approximately 60 pA, with all imaging performed at room temperature.

Analysis of orientation distribution of Sb domains in SEM

A MATLAB-based image analysis algorithm was developed to analyse SEM images of Sb domains. The algorithm detects domain boundaries by processing SEM images and performing a Fourier transform to analyse the orientation of the edges. Edge detection is accomplished using the Canny method with adjustable sensitivity via a graphical user interface. After edge detection, Fourier transform is applied to convert edge information into a spectrum, emphasizing intensity variations. The algorithm calculates the summation of pixel brightness for specific orientation angles within the Fourier transform image, focusing on central features and excluding peripheral noise. The analysis uses a 3° bin size for angle categorization, yielding detailed orientation distribution. Plots visualize orientation angle distribution, facilitating direct comparison. Analysis reveals a marked preference for orientations at 30° intervals, contrasting with less frequent random orientations. Further examination across 60° intervals uncovers two pronounced peaks within each, supporting the hypothesis of important interplay between Sb domain growth dynamics and underlying MoS_2 substrate crystallography. Specific crystallographic directions in the substrate material favour growth orientations at 30° increments, suggesting that deterministic mechanisms guide domain orientation throughout growth and assembly. These findings underscore the pivotal role of substrate crystallography in dictating domain orientation.

DFT calculations

All DFT calculations were performed with the projected augmented wave potentials[61] and the exchange-correlation functional based on the Perdew–Burke–Ernzerhof generalized gradient approximation[62], all implemented in the Vienna Ab-initio Simulation Package[63]. A slab model stacked with monolayer MoS_2 and Sb (01$\bar{1}$2) plane was built to mimic the MoS_2–Sb contact. The supercells of the Sb (01$\bar{1}$2) surfaces and MoS_2 are carefully constructed to ensure the lattice mismatch is less than 3%. A vacuum space >15 Å along the *c* axis was set to avoid spurious interactions between adjacent images. A 400-eV energy cutoff was chosen for the plane-wave basis sets, and the DFT-D3 correction was applied to account for the vdW interactions[64]. All structures were relaxed with a force criterion of 0.02 eV $Å^{-1}$ along with an energy convergence of 10^{-4} eV. Considering the very large systems simulated in

this work, a k-spacing <0.04 Å^{-1} was used for the structural relaxation. For the static electronic structure calculations, the Brillouin zone integrations were sampled on k-spacing <0.01 Å^{-1}. The dipole correction along the c axis of the supercell was considered in all DFT calculations as well. The charge transfer between Sb $(01\bar{1}2)$ and MoS_2 was calculated by Bader charge analysis[65].

Data availability

The data that support the findings of this study are available from the corresponding authors on reasonable request.

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Author contributions

X.W. conceived of and supervised the project. W.L. and X.W. conceived of the idea and designed the experiments. W.L., M.D. and G.X. contributed to transistor fabrication, measurements and data analysis with assistance from C.Z., Z.Y., D.F., H.Q., X.T., N.Z., H.S. and Y.G. F.H. and J.L. performed the transmission electron microscopy and data analysis. W.S. and Y.N. performed XRD and data analysis. X.G., L.M. and J.W. performed the DFT calculations. L.L., X.Z. and T.L. performed chemical-vapour-deposition growth of MoS_2. C.Z., J.X., W.G., Y.S., L.T. and J.-B.X. contributed to discussions and data analysis. W.L., M.D. and X.W. co-wrote the paper with input from other authors. All authors discussed the results and commented on the paper.

Competing interests

The authors declare no competing interests.

Additional information

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